[See Signature Page for Information on Counsel for Plaintiffs]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **PLAINTIFFS' CONSOLIDATED OPENING SUPPLEMENTAL CLAIM CONSTRUCTION BRIEF** **[RELATED CASES]** Date: November 30, 2012 Time: 10:00 a.m. Place: Courtroom 5, 4th Floor Judge: Paul Singh Grewal
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-05398 PSG

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TABLE OF ABBREVIATIONS

'148 patent or '148	U.S. Patent No. 6,598,148, entitled "High Performance Microprocessor Having Variable Speed System Clock," issued July 22, 2003
'336 patent or '336	U.S. Patent No. 5,809,336, entitled "High Performance Microprocessor Having Variable Speed System Clock," issued September 15, 1998
'749 patent or '749	U.S. Patent No. 5,440,749, entitled "High Performance, Low Cost Microprocessor Architecture," issued August 8, 1995
'890 patent or '890	U.S. Patent No. 5,530,890, entitled "High Performance, Low Cost Microprocessor," issued June 25, 1996
Plaintiffs	Declaratory judgment plaintiffs Acer, Inc., Acer America Corporation, Barco, N.V., Gateway, Inc., HTC Corporation and HTC America, Inc.
Defendants or TPL	Declaratory judgment defendants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited
Acer Action	*Acer, Inc., Acer America Corporation and Gateway, Inc. v. Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited*, Civil Case No. 5:08-cv-00877 PSG
Chen Decl.	Declaration of Kyle D. Chen in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief
Talbot	U.S. Patent No. 4,689,581, entitled "Integrated Circuit Phase Locked Loop Timing Apparatus," issued August 25, 1987 to Gerald R. Talbot, Attached as Exhibit

I. INTRODUCTION

Declaratory judgment plaintiffs Acer, HTC and Barco entities, as shown on the caption page (collectively "Plaintiffs"), respectfully and jointly submit this opening supplemental claim construction brief as ordered by the Court. In a previous round of claim construction proceedings, the parties briefed and presented at a *Markman* hearing a set of "top ten" terms. Judge Ware then issued a First Claim Construction Order on June 12, 2012 (Dkt. No. 336, *Acer* Action) ("Order"), in which supplemental briefing was ordered for two of the "top ten" terms: "ring oscillator" and "instruction register." (*See id*. at 16 and 11.)

II. THE CLAIMED "RING OSCILLATOR" MUST BE NON-CONTROLLABLE AND VARY WITH ENVIRONMENTAL PARAMETERS.

The term "ring oscillator" is recited in asserted claims of the '336, '148, '749 and '890 patents. The parties' competing constructions of "ring oscillator" are set forth in the table below:

Plaintiffs' Construction	TPL's Construction
An oscillator having a multiple, odd number of inversions arranged in a loop, **wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment.**	An oscillator having a multiple, odd number of inversions arranged in a loop

At issue in this supplemental briefing is whether the claimed "ring oscillator" should be given a specialized meaning based on the patent owner's arguments made to the PTO during reexamination proceedings. (*See* Order at 14.) In particular, Judge Ware's First Claim Construction Order ordered supplemental declarations and briefing on the meaning of "ring oscillator" in the '336 patent in light of U.S. Patent No. 4,689,581 ("Talbot"). (*See* Order at 16:14–19 ("[Th]e declarants shall fully articulate the technical basis for their opinions with respect to whether the voltage controlled oscillator disclosed in Talbot is or is not a ring oscillator.").)[1]

[1] Judge Ware did not address two related phrases in asserted claims of the '336 patent, in particular "an entire ring oscillator variable speed system clock in said single integrated circuit" (claims 1, 11) and "an entire oscillator disposed upon said integrated circuit substrate" (claims 6, 13), which were fully briefed and argued during the previous *Markman* proceedings. Plaintiffs reserve their right to request construction of these larger phrases following resolution of the construction of "ring oscillator" addressed herein. *See O2 Micro Intern. Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1362–63 (Fed. Cir. 2008) ("When the parties present a

During reexamination of the '148 patent, the PTO cited the Talbot reference as a basis to reject the claims.[2] The applicant responded by clearly and unmistakably distinguishing Talbot's disclosure of a "voltage controlled oscillator (VCO)" from the claimed "ring oscillator," a position TPL continues to assert. (*See* Order at 14–15 (summarizing prosecution history and TPL's arguments).)

Because the patent owner disclaimed Talbot's VCO, the construction of "ring oscillator" cannot read on Talbot's disclosure of any VCO. Plaintiffs' construction properly distinguishes Talbot's "voltage controlled oscillator" in the same way the patent owner distinguished it, by requiring that the "ring oscillator" be non-controllable and variable with the environment. Talbot discloses a "voltage **controlled** oscillator" in Figure 3, and the *control* exerted by the voltage-control circuitry is what distinguishes Talbot from the claimed "ring oscillator."[3]

The "ring oscillator" construction asserted by TPL, and the similar construction tentatively suggested by Judge Ware,[4] are too broad. TPL's construction, "an oscillator having multiple odd inversions arranged in a loop," would read on the "voltage controlled oscillator" in Talbot's Figure 3. As explained in the Supplemental Declaration of Andrew Wolfe and in more detail below, Talbot Figure 3 clearly and unmistakably discloses three inverters arranged in a loop.

A. The Specification Discloses a Microprocessor System Having a Ring Oscillator Variable Speed System Clock.

The specification devotes little more than four paragraphs between columns 16 and 17 to describing the clocking scheme for the claimed microprocessor system. ('336, 16:43–17:10.) The

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fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it.").

[2] Judge Ware found that the '148 patent and the '336 patent are sufficiently related that "any representation regarding similar terms made by the inventors during prosecution of the '148 patent is relevant to its consideration and construction of the terms in the '336 Patent." (Order at 14, n.31.) The arguments made in the text, therefore, should be understood as applying to both the '336 and the '148 patents.

[3] At deposition, TPL's expert testified that the oscillator frequency of Talbot Figure 3 would vary with temperature, voltage and process. (Oklobdzija Depo. at 449:1–17; 467:18–469:18 (Chen Decl., Ex. 1).) Accordingly, the control circuitry is the only remaining distinction.

[4] "Upon review, the Court finds that one of ordinary skill in the art would understand the phrase 'ring oscillator' to mean: 'interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop.'" (Order at 13:20–22.)

only type of circuit disclosed in the specification for providing a clock circuit to a CPU is a "ring oscillator." ('336, 16:56–58.) The specification describes the ring oscillator frequency as non-controllable by virtue of being ***variable*** with environmental parameters.

The specification explains that "[t]emperature, voltage, and process all affect transistor propagation delays." ('336, 16:47–48.) The specification criticizes prior art oscillators used to clock CPUs because they operated at a controlled, but conservatively slow, speed to account for "worse [sic] case" conditions:

> Traditional CPU designs are done so that with the **worse [sic] case** of the three parameters, the circuit will function at the rated clock speed. The result are [sic] designs that **must be clocked a factor of two slower than their maximum theoretical performance**, so they will operate properly in **worse** [sic] **case conditions**.

('336, 16:48–53 (emphasis added).)

The alleged invention purports to overcome these deficiencies with a "ring oscillator" clock that is on the same chip ("die") and made of the same transistors as the CPU it clocks. (*E.g.*, '336, 17:5–7 ("Since the microprocessor 50 ring oscillator clock 430 is made from the **same transistors on the same die** as the latches and gates . . ."") (emphasis added).) The specification touts the claimed ring oscillator's ability to vary in speed with changes in the environmental parameters, thereby compensating for environmental effects on the maximum possible processor speed:

> The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator 430 is useful as a system clock . . . because **its performance tracks the parameters which similarly affect all other transistors** on the same silicon die. **By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast.**

('336, 16:59–17:2 (emphasis added).)

B. TPL Distinguishes the Claimed "Ring Oscillator" from Talbot's VCO at the PTO and Before the Court.

During reexamination of the related '148 patent, TPL emphasized the non-controllability of the claimed clock circuit to overcome prior art. In particular, the Examiner rejected various claims

of the '148 patent based on Talbot. TPL responded by attempting to distinguish Talbot, both during an interview with the examiner and in a later written submission.

With respect to the interview, the Examiner summarized as follows:

> Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator." The patent owner discussed feature of a ring oscillator, such as being **non-controllable, and being variable based on the environment**. **The patent owner argued that these features distinguish over what Talbot teaches.** The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.

('148 PH Interview Summary at 4 of 5, 2/12/08 (Chen Decl., Ex. 2) (emphasis added).)

TPL subsequently submitted a written amendment and remarks that did not include the specific "non-controllable" or "variable based on the environment" arguments that were recounted in the interview summary. TPL instead asserted in conclusory fashion that Talbot fails to disclose a "ring oscillator" because it discloses a "voltage-controlled oscillator (VCO)":

> Further, **Talbot does not teach, disclose, or suggest the ring oscillator** recited in claim 4. The examiner cited col.3, ll. 26-35, and oscillator circuit 12 shown in FIG. 1 of Talbot as teaching the recited ring oscillator. **Talbot discusses a voltage-controlled oscillator (VCO) 12, but does not teach or disclose a ring oscillator.**

('148 PH Remarks/Arguments at 11, 2/21/88 (Chen Decl., Ex. 3) (emphasis added).) TPL did not, however, contradict the interview summary or any of the arguments it made during the interview. As Judge Ware noted, TPL's position remains that Talbot does not disclose a "ring oscillator." (Order at 15:13–15.)

C. The Proper Construction of "Ring Oscillator" Must Not Read on Talbot.

As the Federal Circuit has noted, "[w]here an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of otherwise broad claim language." *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372–73 (Fed. Cir. 2005). In other words, "by distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover, he is by implication surrendering such protection." *Springs Window Fashions LP v. Novo Indus, L.P.*,

323 F.3d 989, 994 (Fed. Cir. 2003) (quoting *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1304 (Fed. Cir. 1997)). This rule is grounded on the principle that "[t]he prosecution history constitutes a public record of the patentee's representations concerning the scope and the meaning of the claims, and competitors are entitled to rely on those representations when ascertaining the degree of lawful conduct." *Id.* at 995.[5]

In this case, the patent owner clearly and unmistakably told the PTO (and the public) that the VCO in "Talbot does not teach, disclose, or suggest the ring oscillator" in order to obtain allowance of claims. ('148 PH Remarks/Arguments at 11, 2/21/88 (Chen Decl., Ex. 3).) TPL cannot now, through subsequent claim construction, obtain a claim scope that reads on the disclaimed Talbot VCO. *See Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1374–75 (Fed. Cir. 2008) ("The doctrine of prosecution disclaimer 'protects the public's reliance on definitive statements made during prosecution' by 'precluding patentees from recapturing through claim interpretation specific meanings [clearly and unmistakably] disclaimed during prosecution.'") (brackets in original) (citation omitted); *see also Desper Prods., Inc. v. Qsound Labs, Inc.*, 157 F.3d 1325, 1340 (Fed. Cir. 1998) ("The public has a right to rely on the assertions made by a patent applicant to secure allowance of its claims. Post-hoc, litigation-inspired argument cannot be used to reclaim subject matter that the public record in the PTO clearly shows has been abandoned.").

D. Plaintiffs' Construction Properly Excludes the Voltage Controlled Oscillator Disclosed in Talbot.

Plaintiffs' construction straightforwardly distinguishes Talbot by simply adopting what the patent owner told the examiner during the interview: that the claimed ring oscillator must be "non-controllable" and variable based on the environmental parameters identified in the specification—namely, temperature, voltage and process. Talbot Figure 3 is an example of a prior art "voltage-

[5] TPL has previously attempted to dismiss its disclaimers to the PTO regarding Talbot by arguing that the Examiner did not rely on them. Even if there was evidence to support this position (which there is not), it is legally irrelevant. *See, e.g., Microsoft Corp. v. Multi-Tech Systems, Inc.*, 357 F.3d 1340, 1350 (Fed. Cir. 2004) ("We have stated on numerous occasions that a patentee's statements during prosecution, whether relied on by the examiner or not, are relevant to claim interpretation.") (citing cases).

controlled oscillator," distinguishable from the claimed "non-controllable" ring oscillator.

Plaintiffs' construction is consistent with the specification of the '336 patent. As explained above, the specification criticizes fixed and controlled prior art CPU clocks as too slow and offers as a purported improvement a ***variable*** speed system clock that always runs at its maximum possible speed. This variable speed clock is "non-controllable" in that it is free to run faster when environmental conditions permit.[6]

Plaintiffs' construction is also entirely consistent with how the applicants described the invention in the original prosecution history of the '336 patent. During the '336 prosecution, the applicants repeatedly drew the distinction between (a) deliberate "control" of the oscillator's frequency through an input signal, crystal or other component of the system and (b) the ability of the oscillator's frequency to vary based on the "environmental parameters" of temperature, voltage and process. For example, in response to rejections of claims reciting a "variable speed clock," a "ring oscillator variable speed system clock" and an "oscillator," the applicants made the following arguments:

> **A <u>ring oscillator</u> will oscillate at a frequency determined by its fabrication and design and the operating environment**. Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. **Crucial to the present invention is that** since both the oscillator or variable speed clock and driven device are on the same substrate, **when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in** that the oscillator or variable speed clock and the driven device are on the same substrate, and **that the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so**.

('336 PH Amendment at 5, 07/07/97 (Chen Decl., Ex. 4) (emphasis added).)

The patent owner continued to draw this "crucial" distinction between the prior art's

[6] At deposition, Dr. Oklobdzija agreed that the ring oscillator disclosed by the '336 patent is "free running." (Oklobdzija Depo. at 413:16-416:2 (Chen Decl., Ex. 1).)

concept of "control" (*e.g.*, based on manual or programmed inputs or external components) and the environmental factors discussed in the patent. For example, the patent owner contrasted the "frequency controlled" clock in U.S. Patent No. 4,503,500 ("Magar") with the claimed "variable speed clock," "ring oscillator variable speed system clock" and "oscillator" as follows:

> [O]ne of ordinary skill in the art should readily recognize that **the speed of the cpu and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature** of the IC in the Magar microprocessor . . . . This is simply because the **Magar microprocessor clock is frequency <u>controlled</u> by a crystal** which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. **The Magar microprocessor in no way contemplates a variable speed clock as claimed**.

(*Id.* at 3–4 (italics in original; boldface and underlining added).) The patent owner further argued:

> **The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature** in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.

(*Id.* at 4 (emphasis added).)

In another example, the patent owner distinguished the "frequency control information" and "clock control signals" in U.S. Patent No. 4,670,837 ("Sheets") from the claimed variable speed clocking mechanisms:

> **The present invention <u>does not</u> similarly rely upon provision of frequency <u>control</u> information to an external clock**, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of **frequency control information** described by Sheets, since **the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance**. Sheets' system for providing **clock control signals** to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

('336 PH Amendment at 8, 04/15/96 (Chen Decl., Ex. 5) (emphasis added).)

Specifically, the patent owner pointed out that the claimed oscillator will "naturally tend to vary commensurately in speed as a function of **various parameters (*e.g.*, temperature)** affecting circuit performance." *Id.* (emphasis added). Later, the patentee went even further to distinguish Sheets' clock "in the same integrated circuit" controlled by a "command input" as follows:

> Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. **In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency**.

('336 PH Amendment at 4, 01/03/97) (Chen Decl., Ex. 6) (emphasis added).)

Having already characterized the claimed "ring oscillator" as environmentally dependent, and having already expressly distinguished it from prior art clocks that were "controlled," whether through "clock control signals," "frequency control information," or "command inputs," the patent owner's disclaimer during reexamination can be seen as simply reiterating the same "features of a ring oscillator, such as being non-controllable, and being variable based on the environment" to distinguish the claims over the prior art. ('148 PH Interview Summary at 4 of 5, 2/12/08 (Chen Decl., Ex. 2).)

E. TPL's Construction Must Be Rejected Because It Reads on Talbot.

TPL now seeks to accuse the same type of voltage-controlled clocks it had to disclaim during prosecution and reexamination. (*See* Chen Decl., Ex. 7.) It would be improper to permit this. *See Computer Docking*, 519 F.3d at 1374–75 (Fed. Cir. 2008) ("precluding patentees from recapturing through claim interpretation specific meanings [clearly and unmistakably] disclaimed during prosecution.") (brackets in original) (citation omitted); *see also Desper Prods.*, 157 F.3d at 1340 ("Post-hoc, litigation-inspired argument cannot be used to reclaim subject matter that the public record in the PTO clearly shows has been abandoned."). Thus, the claimed "ring oscillator" must be given a specialized construction that expressly incorporates the "non-controllable"

disclaimer. In light of the foregoing, Plaintiffs respectfully request that the Court construe "ring oscillator" as "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment."

TPL's proposed construction and the tentative construction offered by the First Claim Construction Order must both be rejected because they read on the "voltage-controlled oscillator" of Talbot Figure 3. Those constructions require nothing more than an "oscillator" that has three inversions/inverters[7] arranged in a loop. To avoid its disclaimers to the PTO, TPL has asserted in this litigation that the "voltage-controlled oscillator" of Talbot does not meet this broad definition, but TPL is wrong. As explained in the Supplemental Wolfe Declaration (Chen Decl., Ex. 8), Talbot reads directly on TPL's proposed construction. Dr. Wolfe's declaration identifies where the three inversions/inverters are in Talbot, identifies the loop traversed by the oscillation signals, and cites multiple credible references to support characterizing each identified inversion as an "inverter."

Specifically, the Supplemental Wolfe Declaration includes an annotated Talbot Figure 3, reproduced below, showing the following three inverters: (1) inverter 51; (2) transistor pair 48 and 49; and (3) inverting type Schmitt-trigger 52. (Supp. Wolfe Decl. at 3 (Chen Decl., Ex. 8).) It also shows the path of the oscillation signals around the loop formed by the three inverters

There cannot be any dispute that feature 51 of Talbot Figure 3 is an inverter, because Talbot describes it as "inverter 51." (Talbot at 7:51 (Chen Decl., Ex. 9).) At deposition, TPL's expert Dr. Oklobdzija agreed with the obvious: inverter 51 is an inverter. (Oklobdzija Depo. at 436:16–437:3 (Chen Decl., Ex. 1).)

Dr. Wolfe's characterization of transistor pair 48 and 49 as an inverter is supported by diagrams from multiple textbooks, including a textbook co-authored by Dr. Oklobdzija. (Supp.

[7] Although the First Claim Construction Order used the term "inverter" instead of TPL's proposed term "inversion," there was no evidence presented to or cited by the Court to support a distinction between the words. At deposition, both experts indicated that there could be "inversions" that are not "inverters," but Dr. Wolfe's declaration explains that the "inversions" of Talbot Figure 3 are in fact "inverters," so the distinction does not matter to Dr. Wolfe's analysis.

Wolfe Decl. at 4–6 and Ex. L (Chen Decl., Ex. 8).)

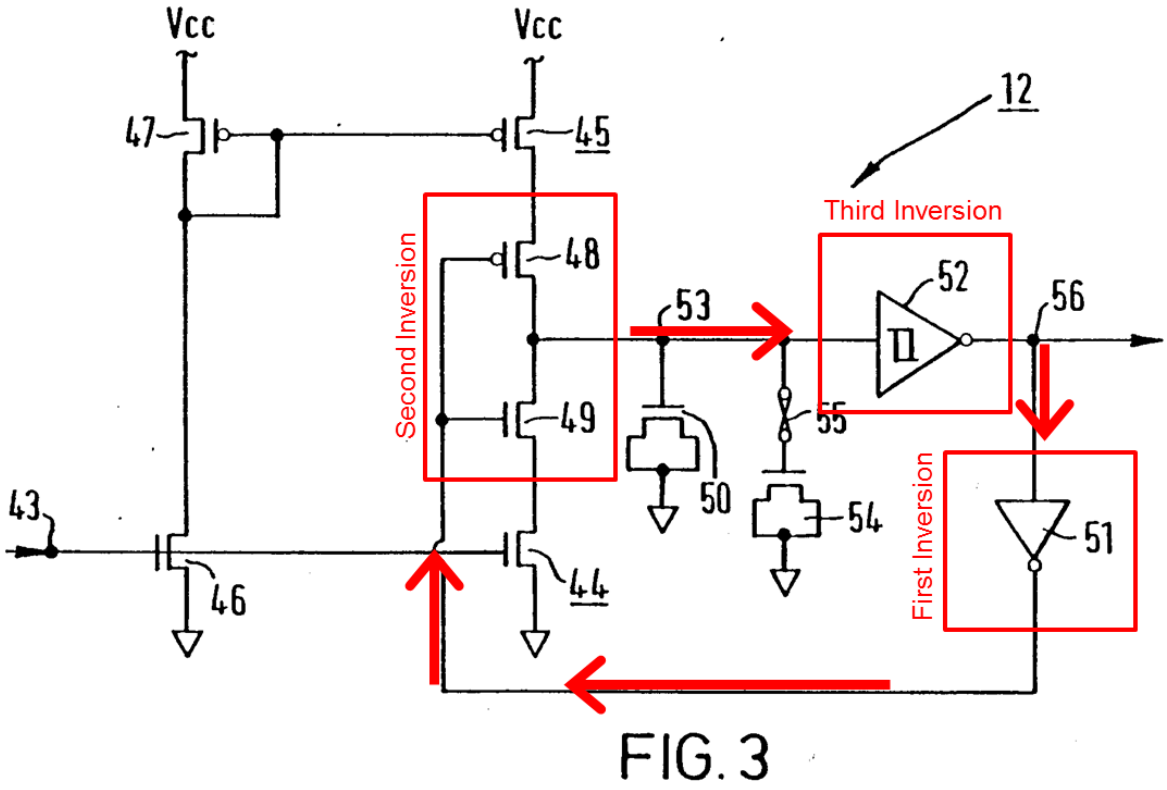

FIG. 3

Dr. Wolfe's declaration explains that an inverting type "Schmitt-trigger" has "hysteresis" on its input, meaning that instead of a single threshold, the Schmitt-trigger has two thresholds for changing its output, one for a rising input signal and one for a falling input signal, respectively. This feature that helps make the inverter's output less sensitive to noise on the input. (*Id.* at ¶¶ 15–16.) Dr. Wolfe's characterization of an inverting type Schmitt-trigger as an inverter is supported by the text of Talbot, which explicitly states that the output of Schmitt-trigger 52 is high when its input is low. (Talbot, 7:67-8:1 (Chen Decl., Ex. 10).) It is also supported by numerous datasheets describing commercially available inverters having Schmitt-trigger inputs. (Supp. Wolfe Decl. at ¶¶ 17–21 and Exs. D, E, F, G (Chen Decl., Ex. 8).) It is further supported by patents directed to "Schmitt-trigger inverters." (*Id.* at ¶ 22 and Exs. H, I.) Finally, it is supported by Exhibit A to Dr. Oklobdzija's supplemental declaration, which includes a slide that explicitly captions the very symbol used for Talbot Figure 3's feature 52 as a "Schmitt-trigger inverter." (Supp. Oklobdzija Decl., Ex.A at slide 3 (Chen Decl., Ex. 17).)

Thus, because there are three inverters connected in a loop as disclosed in Figure 3 of Talbot, TPL's proposed or the Court's tentative constructions read on the VCO as disclosed in Figure 3 of Talbot, notwithstanding the additional circuitry providing *control*. *E.g.*, *Free Motion Fitness, Inc. v. Cybex Intern., Inc.*, 423 F.3d 1343, 1353 (Fed.Cir. 2005). Because TPL has clearly and unmistakably disclaimed the VCO in Talbot, neither TPL's proposed nor the Court's tentative construction should be adopted. *See Computer Docking*, 519 F.3d at 1374–75 (Fed. Cir. 2008); *see also Desper Prods.*, 157 F.3d at 1340.

F. Dr. Oklobdzija's Supplemental Declaration Does Not Address the Issue.

Dr. Oklobdzija's supplemental declaration fails to address the issue. Although he argues that Talbot does not disclose a "ring oscillator," he does not specify the construction of "ring oscillator" applied to distinguish Talbot. Indeed, Dr. Oklobdzija's supplemental declaration does not address any of the proposed constructions of "ring oscillator". (Oklobdzija Depo. at 406:11–407:14 (Chen Decl., Ex. 1).) Dr. Oklobdzija testified that he prepared his supplemental declaration without having reviewed the '336 patent for two years. (*Id.* at 411:9–21.)

Dr. Oklobdzija's supplemental declaration does not deny that Talbot Figure 3 discloses three inverters in a loop. In fact, Dr. Oklobdzija's supplemental declaration does not analyze Talbot Figure 3 at all. Rather than analyze Talbot Figure 3, Dr. Oklobdzija analyzes a different, hypothetical circuit that includes only the Schmitt-trigger 52 and input capacitors, *and an additional direct connection between the Schmitt-trigger 52's input and the output that is not present in Talbot*. This is non-responsive to what Judge Ware directed—that the parties specifically address the oscillator in Talbot, not a different and hypothetical circuit. His analysis is also irrelevant because it is *not* on Talbot.

III. THE OPERANDS, IF PRESENT IN THE CLAIMED "INSTRUCTION REGISTER," MUST BE RIGHT JUSTIFIED.

A microprocessor generally operates by executing "instructions" that direct the microprocessor to perform specific operations. An instruction can include two components: (1) an "opcode" and (2) an "operand." The "opcode" or operation code specifies the specific operation

the instruction is intended to perform. The values on which the specified operation will be performed are referred to as "operands." Using an analogy to the mathematical expression (5 + 3), for example, the opcode is "+" and the two operands are the values "5" and "3." (May Decl. at ¶¶ 4–6 (Chen Decl., Ex. 18).)

An "instruction register," generally speaking, is a storage device that holds one or more instructions and supplies those instructions to the microprocessor circuits responsible for their interpretation and execution. An instruction register may be of different widths or sizes, measured by the number of "bits" it can hold. A "bit" in computer science is a unit of information that specifies a value of either 1 or 0, and the term "byte" refers to a unit of information that includes 8 bits. The specification of the '749 patent, for example, discloses an instruction register that can hold up to 32 bits (4 bytes) of instructions (*i.e.*, a 32-bit instruction register). (*Id.* at ¶ 7.)

As explained in detail below, the '749 patent describes a highly specialized microprocessor system that features a unique type of "instruction register" that arranges the operands in a particular manner. The parties' proposed constructions for the term "instruction register" are set forth below:

Plaintiffs' Construction	TPL's Construction
register that receives and holds one or more instructions for supplying to circuits that interpret the instructions**, in which any operands that are present must be right-justified in the register**	register that receives and holds one or more instructions for supplying to circuits that interpret the instruction

The sole dispute between the parties turns on whether the operands present in the instruction register must be right justified. Judge Ware declined to reach this issue in the First Claim Construction Order and directed the parties to brief whether a statement made in an interview summary in the prosecution history of the '749 patent (*i.e.*, "operand width is variable and right adjusted") supports such a requirement. (Order at 11 n.23.)

The '749 specification explains that instructions can be of "variable" width or size. While the opcode of an instruction is generally 8 bits (one byte) wide, an operand when present may be 8, 16 or 24 bits (one, two or three bytes) wide—resulting in an instruction width of 16, 24 or 32 bits (two, three or four bytes), respectively. ('749, 18:34–56.) This variable-width characteristic

means that instructions will not always be positioned in the same place in a 32-bit instruction register, meaning that the operands may be placed in different locations within the instruction register. This variability requires additional circuitry in the microprocessor system to locate the operand among several different possible positions such that the microprocessor "knows" what to use as the "opcode" and what to use as the "operand" during an operation. (May Decl. at ¶¶ 8–10, 13 (Chen Decl., Ex. 18).) As shown below, the '749 patent avoids this problem by requiring that the operand be "right justified" in the instruction register.

The term "right justified" refers to the fact that an operand of an instruction is always positioned in the "right side" of the instruction register. The figures below demonstrate this concept. In each of these examples, a 32-bit (4-byte) instruction register such as the one described in the '749 patent is broken into four bytes of eight bits each, which are shown side-by-side from left to right. (*Id.* at ¶¶ 9–10.) The two examples below show operands of different widths that are always located in the right-most bits of the instruction register:

Examples of "right justified" operands in a 32-bit instruction register

Right justified 8-bit (1-byte) operand:

8 bits	8 bits	8 bits	8 bits
Opcode	Opcode	Opcode	**Operand**

Left bit 32-bit Instruction Register Right bit

In the example above, the 32-bit instruction register contains two 8-bit instructions towards the left side, each of which has only an 8-bit opcode without any operand, and then a 16-bit instruction with an 8-bit opcode and an 8-bit operand that is positioned in the "right side" of the instruction register.

Right justified 16-bit (2-byte) operand:

8 bits	8 bits	8 bits	8 bits
Opcode	Opcode	**(part of the) Operand**	**(part of the) Operand**

Left bit 32-bit Instruction Register Right bit

In the example above, the 32-bit instruction register contains one 8-bit instruction towards the left side, which has only an 8-bit opcode without any operand, and then a 24-bit instruction with an 8-bit opcode and a 16-bit operand that is positioned in the "right side" of the instructionregister.

Because a microprocessor needs the entire operand to execute an instruction correctly, it needs to be able to determine precisely where the operand begins and ends—in other words, the width of the operand. One approach in microprocessor design that is expressly criticized in the '749 patent is to use a different opcode for each possible operand length. For example, a common microprocessor instruction described in the '749 patent is known as a "JUMP" instruction, which tells the microprocessor to begin executing instructions at a different location in the memory, or "address." Because the operand of a JUMP instruction is used to determine the precise address to which the microprocessor will jump, the operand length may vary based on whether the target address is close to, or far away from, the current location. In either case, the "opcode" must specify both the JUMP instruction and the width of its corresponding operand, *e.g.*, 8, 16 or 24 bits. The opcode, for example, would need to tell the microprocessor, "this is a JUMP instruction and the opcode length is 16 bits." The disadvantage of this approach is that, in this example, three separate opcodes would be required for the same JUMP operation to account for three possible operand lengths. (May Decl. at ¶¶ 10–11 (Chen Decl., Ex. 18).)

The "right justified" instruction register in the '749 patent avoids this issue entirely by placing all of the bytes of the operand (up to 3) on the right-side of the instruction register, and placing the opcode of the instruction immediately to the left of the operand bytes, as shown in the figures above. Execution of the instructions proceeds from left-to-right of the instruction register, causing the opcode to be encountered first. The operand is then obtained by simply reading it from the right-most bits of the instruction register until before the opcode. Because the operands are "right justified" and therefore always located in the same place in the instruction register, there is no need to rely on the opcode to determine the operand width. (*Id.* at ¶¶ 11–12.) And because the opcode no longer needs to specify the width or size of the operand, this "right justified"

approach allows the same opcode to be used for a particular operation regardless of the operand width. As explained in the specification:

> Variable Width Operands
>
> Many microprocessors provide variable width operands. The microprocessor **50** handles operands of 8, 16, or 24 bits using the same op-code. FIG. 20 shows the 32-bit instruction register **108** and the 2-bit microinstruction register **180** which selects the 8-bit instruction. Two classes of microprocessor **50** instructions can be greater than 8-bits, JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter **180** selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder **440** and gates **442**. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

('749, 18:34–56 (emphasis added).)

The passage above describes the ability to handle variable width operands using the same opcode as "magic" and proclaims, "This magic is possible because **operands must be right justified in the instruction register**. This means that the least significant bit of the operand is **always** located in the least significant [*i.e.*, right-most] bit of the instruction register." ('749, 18:43–47 (emphasis added).) This passage makes clear that right justifying operands in the instruction register is not simply an optional design choice of an embodiment in the specification, but a required characteristic—something that "must be" and "always is" present, to accomplish the "magic" of the alleged invention.

It is within this context that the statements in the '749 prosecution history are best understood. The importance of the "magic" described in the specification was emphasized in response to an Office Action rejecting several pending claims over U.S. Patent No. 5,127,091 to Boufarah. In a summary of an in-person interview with the examiner on October 25, 1994, the examiner noted with respect to claim 1, "operand width is **variable** and **right adjusted**." ('749

PH Interview Summary at 1, 10/25/94 (Chen Decl., Ex. 19) (emphasis added).) The prosecution history does not reveal the circumstances in which this statement is made, and no transcript of the interview is available. The interview summary nonetheless tracks the specification's description of "variable width" operands and the requirement of right justified operands in the instruction register.

It is expected that TPL will argue, as it did before Judge Ware, that its statements in the specification and the statement reflected in the interview summary cannot limit "instruction register" because they do not rise to the level of a clear and unequivocal disclaimer. But TPL is wrong. The Federal Circuit has repeatedly held that a narrower construction may be adopted "if the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention." *Edwards Lifesciences, LLC v. Cook Inc.*, 582 F.3d 1322, 1329 (Fed. Cir. 2009) (citation omitted). The applicants described the use of right-justified operands in the instruction register with clear and mandatory language, and criticized prior art microprocessors that did not have right justified operands. *See SciMed Life Systems, Inc. v. Advanced Cardiovascular Systems, Inc*., 242 F.3d 1337, 1341 (Fed. Cir. 2001) ("Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question."). Accordingly, for the reasons stated above, Plaintiffs' proposed construction should be adopted.

IV. CONCLUSION

For the foregoing reasons, Plaintiffs' constructions should be adopted in their entirety.

Dated: October 19, 2012

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ATTESTATION PER GENERAL ORDER 45

I, Kyle D. Chen, am the ECF User whose ID and password are being used to file Plaintiffs' Consolidated Responsive Claim Construction Brief. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

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